Sixty-GHz-Band Ultra-Miniature Monolithic T/R Modules for Multimedia Wireless Communication Systems

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Abstract— **The development of 60 GHz-band ultra-miniature FM/frequency-shift keying (FM/FSK) transmitter/receiver modules fabricated with a complete monolithic-microwave integrated circuits (MMIC) chip set, including dielectrically stabilized fundamental-frequency oscillators for multimedia wireless communication systems, is reported. The 0.9 cc transmitter module, which consists of a voltage controlled oscillator (VCO) and two power amplifiers, exhibits 11.5 MHz/V modulation sensitivity, 10.2 dBm output power, and −2.4 ppm/°C frequency stability. With the receiver module, which consists of low noise amplifier (LNA), a mixer, and a local oscillator (LO), 5.4 dB double-side band (DSB) noise figure with 10.8 dB downconversion gain has been achieved. The 60 GHz-band monolithic dielectric-resonator (DR) stabilized oscillators offer a practical approach to ultra-miniature transmitter/receiver modules for high-speed wireless LAN systems with data rates greater than 10 Mbps and for video-signal and compressed HDTV-signal (MUSE) transmission systems.**

I. Introduction

THERE HAVE been increasing demands for transmitting multimedia information using high-speed digital data and wide-band image signals, such as video and high definition television (HDTV) signals, through compact and handy systems. Wireless communication systems in the 60 GHz-band are useful for such applications because of their high potential for realizing compact size, easy beam forming, and wide bandwidth. The 60 GHz-band is ideal for picocell zoning, owing to high atmospheric attenuation loss of the radiated signals [1], [2]. For the 60 GHz-band, monolithic-microwave integrated circuits (MMIC's) for communication and sensing systems have been developed [3]–[17]. Furthermore, the development of millimeter wave modules for system applications at 60 GHz-band and above has been focused on amplifier modules [5], [18], [19], multiplied frequency-source modules [20], [21], and a receiver module including a multiplied frequency-generation MMIC chip [22]. However, practical complete transmitter/receiver (T/R) modules of compact size have not been reported yet. This paper reports on the development of 60 GHz-band ultra-miniature T/R modules, which utilize a complete monolithi-IC chip set for high-speed wireless LAN's and video-signal transmission systems. The specific feature of the T/R modules is the use of 60 GHz MMIC fundamental-frequency oscillators stabilized with a dielectric resonator (DR), which are a voltage controlled oscillator (VCO) as an FM/frequency-shift keying (FM/FSK) modulator for the transmitter and a local oscillator (LO) for the receiver, realizing very simple and compact modules.

The RF circuit configuration, MMIC technologies, 60 GHz-band MMIC chip set, T/R module structures, and their performances are described. The 0.9 cc FM/FSK T/R modules have demonstrated high performance applicable to practical multimedia wireless communication systems.

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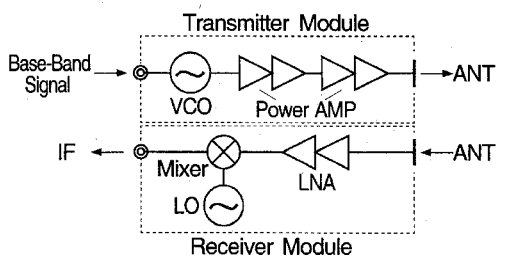

Fig. 1. Block diagram of the 60 GHz-band transmitter and receiver modules.

II. RF Circuit Configuration

The block diagram of the RF front-ends is shown in Fig. 1. This configuration is appropriate for the minimum delay spread (MDS) LAN and direct-beam video-signal transmission system, avoiding problems associated with multipaths and a propagation delay to lead to the elimination of route diversities [23]. The circuit configuration is very simple, can be fabricated in a compact size, and is effective to reduce the cost of millimeter wave systems. The transmitter module consists of a VCO as an FM/FSK modulator and two power-amplifiers.

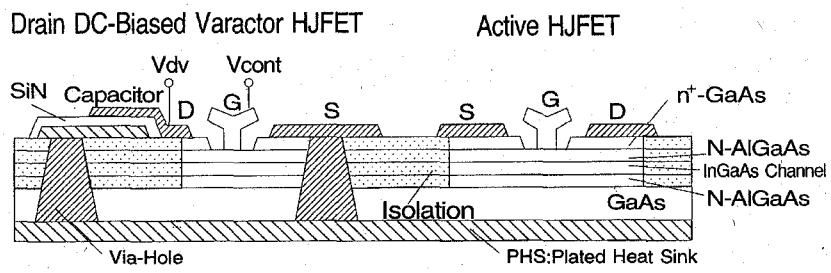

Fig. 2. Cross-sectional view of the MMIC VCO. The right part is an active HJFET. The left part is an integrated varactor HJFET.

The final amplifier-block acts as a burst on/off switch in LAN operation, which is required to have high isolation, as well as an output amplifier. The output power and frequency stability are designed to be 10 dBm (10 mW) and within ± 100 ppm for the ambient temperature of $25 \pm 15°C$, respectively, for indoor communication use. The receiver module, which is a down-converter, consists of a low noise amplifier (LNA), a mixer, and a stabilized LO. The IF is nominally set at 500 MHz.

III. MMIC Chip Set

A. MMIC Technologies

A 60 GHz-band MMIC chip set for wireless communication systems has been developed based on 0.15-μm gate N–AlGaAs/InGaAs heterojunction FET (HJFET) MMIC technologies. Fig. 2 shows the device structure including an integrated varactor for the MMIC VCO. An N–AlGaAs/InGaAs/N–AlGaAs double heterojunction FET (DH-HJFET) as shown in the right part of the figure, which has a high drain current with a high breakdown voltage compared to the single heterojunction FET, is used as an active element. The Al content of the N–AlGaAs layer is 0.22, which is less than 0.3 for the conventional N–AlGaAs/GaAs system, to reduce DX centers, and the pinch-off voltage is deeper than -2 V so as to obtain a high drain current and for the channel to not be affected from the surface effects, so that the main origins of the 1/f noise are reduced. The In content of the InGaAs channel layer is 0.2. The sheet doping concentrations in the upper and lower N–AlGaAs layers are 3.6×10^{12} cm^{-2} and 1.8×10^{12} cm^{-2}, respectively. The spacing between the gate and drain recess edge of the HJFET was optimized to be 0.4 μm for high gain, high maximum drain current (Imax), and high gate breakdown voltage (BVgd), simultaneously. The HJFET with a 100-μm-wide gate (50 μm $\times$ 2) has a high fmax of more than 220 GHz with 500–700 mA/mm Imax and higher than 10 V BVgd [4], [14]. For frequency modulation in the VCO, a drain dc-biased HJFET is integrated as a varactor as shown in the left part of Fig. 2. Fig. 3 shows CV curves for the gate of the varactor HJFET. A drain dc-bias of about 0.5 V brings smooth change in the gate capacitance with gate voltage, which is effective for linear frequency control [24]. Without the drain bias, the gate capacitance sharply decreases near the pinchoff with negative gate voltage due to full depletion of the channel. With the drain bias, on the other hand, a part of the channel at the drain side is already depleted, and the channel gradually becomes fully depleted with a negative gate voltage, resulting in the gradual decrease of the gate capacitance.

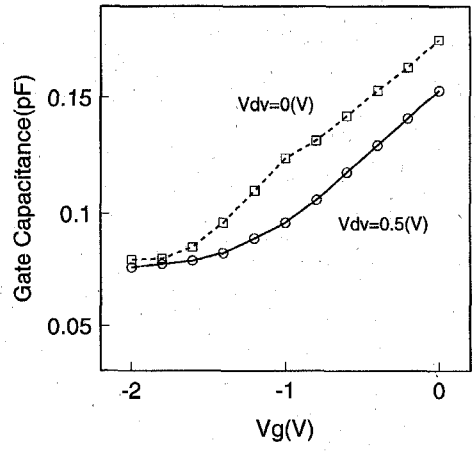

Fig. 3. CV characteristics of the gate capacitance of the varactor HJFET with the drain bias as a parameter.

The circuits are based on a microstrip-line configuration. The GaAs substrate thickness is 40 μm, and the plated heat sink (PHS) is adopted for high-power handling capability. All groundings are made through 30-μm square via-holes. Metal–insulator–metal (MIM) capacitors of 3 pF with a SiN dielectric film are used for bypass and dc-cut capacitors. The circuits were designed for practical use in wireless communication systems with a number of the frequency carrier. The amplifiers were designed to have wide-band operation capability as well as high stability. The oscillators are assembled with a high Q dielectric resonator (DR) directly attached on the MMIC chip for high frequency stability and low phase noise. The oscillation frequency can be mechanically tuned and adjusted to the desired value of the application system using a fine screw placed above the DR.

B. Voltage-Controlled Oscillator Chip

A VCO chip is shown in Fig. 4. The oscillator circuit has shorted stubs connected to the source electrodes of the active HJFET as the series feedback elements. A drain dc-biased HJFET varactor is connected to the gate of the active FET. The oscillation is stabilized with a DR to achieve low phase noise and high stability with temperature. A rod-shaped $TE_{01\delta}$-mode DR made from $Ba(Mg, Ta)O_3$ is directly attached onto the MMIC chip. The product of the unloaded Q and frequency of the DR itself is 320 000 GHz, which is the highest level among dielectric ceramics. A single-stage wide-band buffer-amplifier

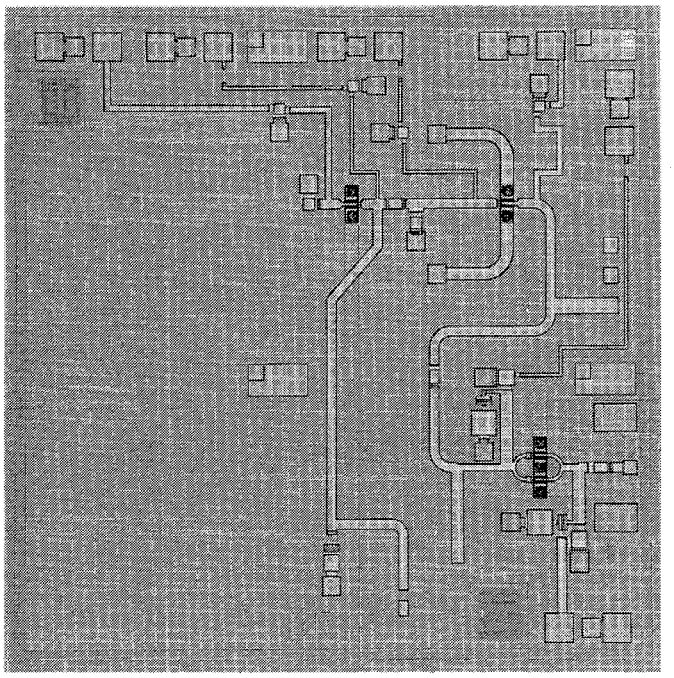

Fig. 4. Microphotograph of the 60 GHz-band MMIC VCO chip. This shows the chip before attaching a DR. The chip size is 2.22 × 2.22 mm^2.

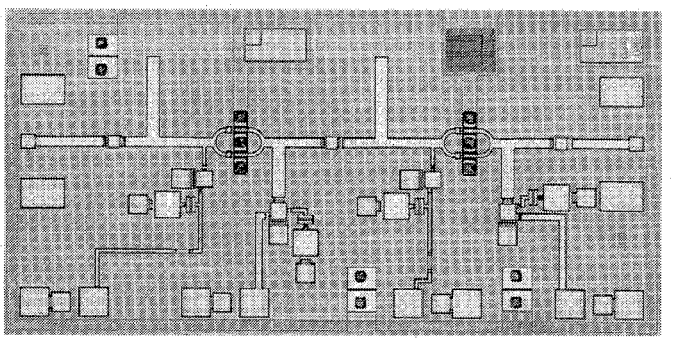

Fig. 5. Microphotograph of the 60 GHz-band two-stage wide-band power-amplifier chip. The chip size is 1.07 × 2.22 mm^2.

with a 200-μm (50-μm × 4) wide HJFET is jointly integrated within the same chip to achieve high output power and better external interface. The buffer-amplifier is one stage of the two-stage wide-band power amplifier described in the next paragraph. The chip size is 2.22 × 2.22 mm^2. A modulation sensitivity of 55 MHz/V and an output power of 6.9 dBm with a phase noise of −80 dBc/Hz at 100 kHz off-carrier have been obtained at 60.0 GHz for a 0.5 V drain bias of the varactor HJFET. The frequency pushing for the drain voltage of the buffer amplifier is only 1.4 MHz/V [13].

C. Power-Amplifier Chip

Fig. 5 shows a two-stage wide-band power-amplifier chip [16]. A 200-μm (50 μm × 4) wide HJFET is used for both the first stage and second stage. The specific features of this amplifier are a wide frequency-band operation using compact matching circuits based on a shorted stub [25] and high stability obtained by incorporating a resistance-capacitance (RC) network in the bias-line and an open stub in the input matching circuit. The short-length matching circuit elements

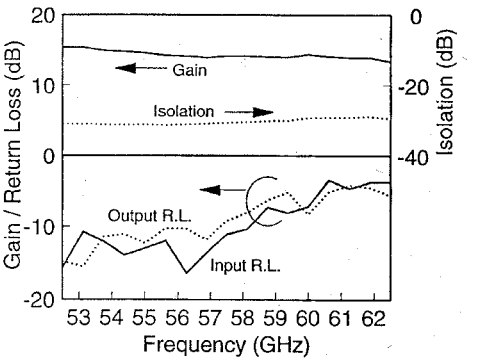

Fig. 6. Small-signal frequency response of the two-stage wide-band power-amplifier. The drain bias is 2.5 V.

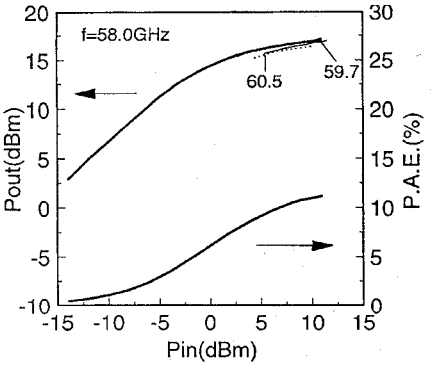

Fig. 7. Power input to output characteristics of the wide-band amplifier. The drain bias is 4.25 V.

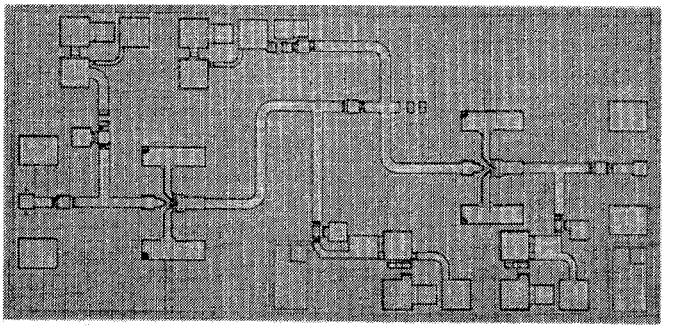

Fig. 8. Microphotograph of the 60 GHz-band LNA chip. The chip size is 1.07 × 2.22 mm^2.

have small phase-deviations with frequency, resulting in wide-band operation capability. The chip size is 1.07 × 2.2 mm^2. The small-signal frequency response of the MMIC amplifier is plotted in Fig. 6. The amplifier exhibits a very flat gain of 14 dB over the frequency from 52.5 GHz–62.5 GHz with a high isolation of 30 dB. Fig. 7 shows the power performance. The output power is higher than 16.5 dBm at 7 dB gain. The maximum output power is 17.1 dBm, and the power-added efficiency is 11.5% at 58 GHz. The power density is 0.26 W/mm. The developed amplifier is suitable for various applications such as buffer amplifiers and output amplifiers for indoor transmission systems.

D. Low-Noise Amplifier Chip

Fig. 8 is a two-stage LNA chip photograph. The matching circuit consists of a transmission line and a shorted stub. The

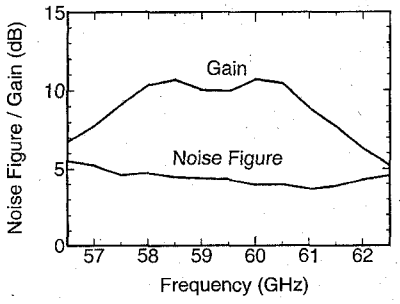

Fig. 9. Frequency responses of the LNA noise figure and gain. The drain bias is 2.0 V.

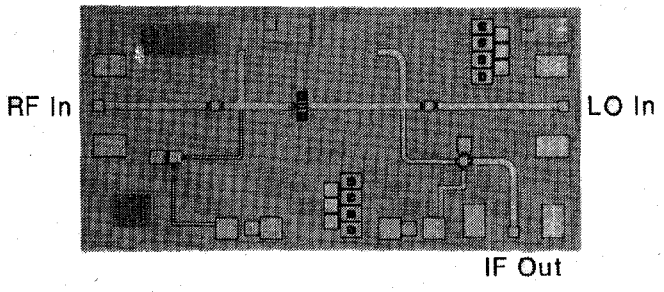

Fig. 10. MMIC drain-mixer chip. The chip size is 1.07 × 2.22 mm^2.

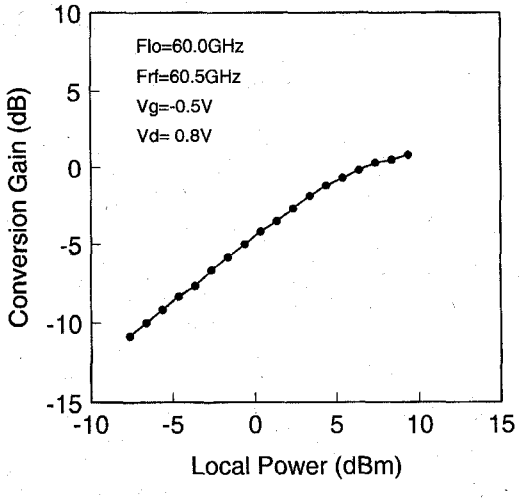

Fig. 11. Drain-mixer conversion gain versus LO power.

LNA was designed to attain flat high-gain and stable operation by optimizing the interstage matching circuit and *RC* network in the bias line. The chip size is 1.07 × 2.22 mm^2. Fig. 9 respresents the frequency response of the noise figure and gain of the LNA. The LNA exhibits a 10.3 ± 0.4 dB gain with less than 4.7 dB noise figure from 57.8–60.7 GHz. A minimum noise figure of 3.9 dB is obtained at 59.5 GHz.

E. Mixer Chip

Fig. 10 shows a single-ended drain-mixer chip. The RF signal is applied to the HJFET gate, and the LO signal is applied to the drain. The IF signal is taken from the drain. Therefore, the drain-mixer has an advantage of easy isolation of the RF signal from the LO signal, resulting in a simple circuit configuration. The chip size is 1.07 × 2.22 mm^2. The

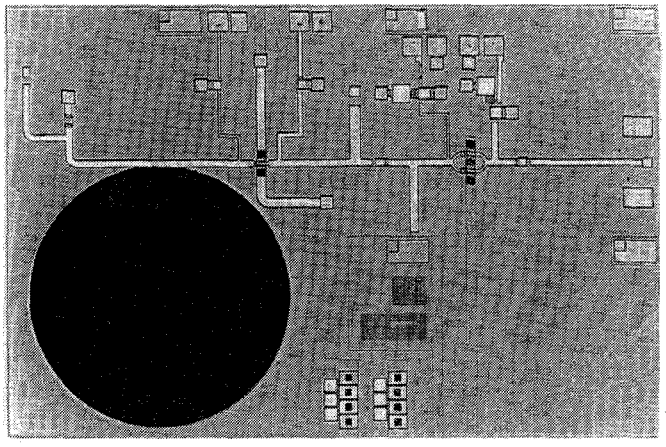

Fig. 12. MMIC LO photograph. DR is attached directly onto the MMIC chip. The chip size is 2.22 × 3.37 mm^2.

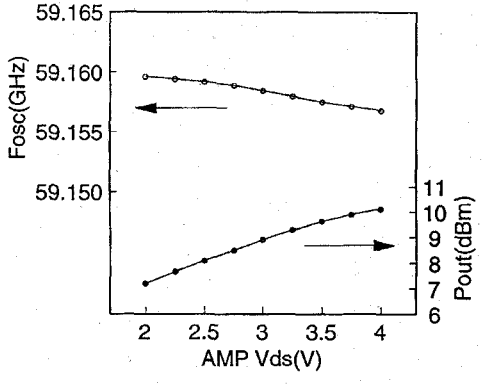

Fig. 13. LO output power and frequency dependences on the drain voltage of the buffer-amplifier.

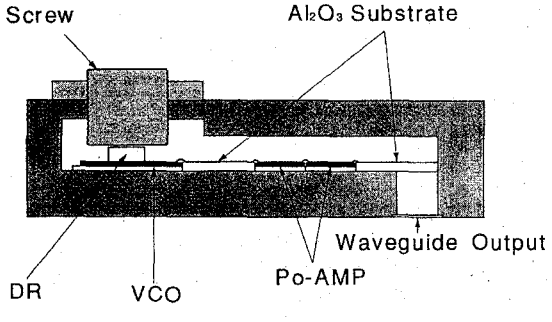

Fig. 14. Schematic diagram of the transmitter module; cross-sectional view.

mixer was designed to be biased in highly nonlinear operation in order to obtain high conversion gain. The drain is swung by the LO signal, so that the drain bias is set around the knee voltage in Id–Vd characteristics of the HJFET. The relationship between the IF power and LO power for the mixer is plotted in Fig. 11. The RF power is −20 dBm. The mixer has a conversion gain of 0.5 dB at 60.5 GHz for 7 dBm applied LO power and 500 MHz IF output. This represents the state-of-the-art performance for an MMIC drain-mixer in this millimeter-wave frequency range.

F. Local Oscillator Chip

Fig. 12 is a LO photograph [16]. The LO consists of a dielectric resonator oscillator (DRO) and a co-integrated

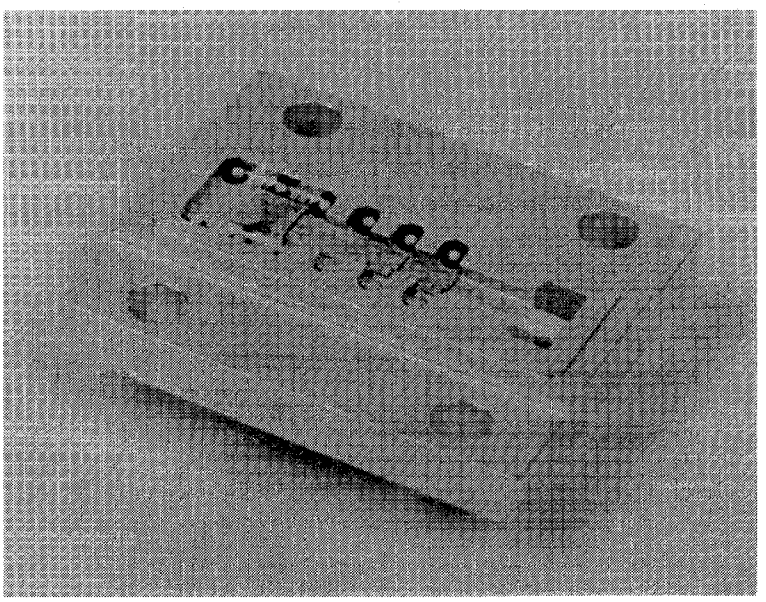

Fig. 15. Transmitter module photograph. This shows the main body without the cap.

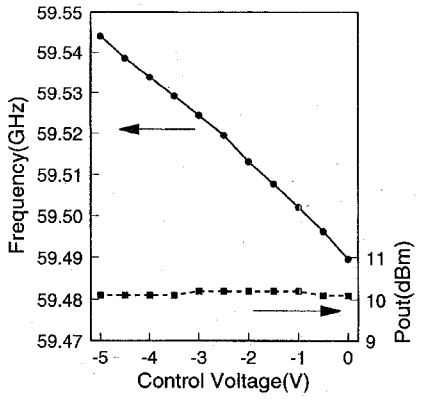

Fig. 16. Transmitter module output frequency and power variations with control voltage.

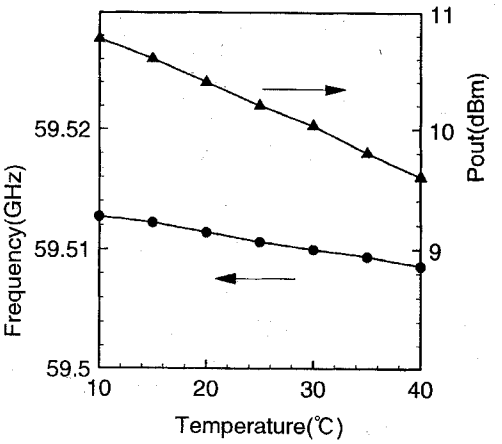

Fig. 17. Temperature dependence of the transmitter module output frequency and power.

single-stage wide-band buffer-amplifier. The oscillator circuit has a series feedback topology using shorted stubs connected to the source electrodes of the active HJFET as feedback elements. The chip size is 2.22×3.37 mm^2. The LO exhibits the state-of-the-art performance for transistor oscillators operating above 40 GHz. In Fig. 13 the output power and frequency are plotted versus the drain bias of the buffer-amplifier. High output power of 10.1 dBm has been achieved. The frequency pushing is only 1.4 MHz/V. Furthermore, low phase noise of -90 dBc/Hz at 100 kHz off-carrier is obtained at 59.157 GHz. The frequency stability is high with a small temperature coefficient of 1.6 ppm/°C, which is comparable to or better than that for Ka-band DRO's reported so far [8], [26], [27]. This LO performance is well matched to the drain-mixer.

IV. Transmitter/Receiver Modules

A. Transmitter Module

The cross-sectional structure of the transmitter module is illustrated in Fig. 14, and a fabricated module is shown in Fig. 15. A VCO chip and two power-amplifier chips are mounted in a metal package with a microstrip-line/waveguide transition. The transition and interconnection lines between the chips are formed on Al_2O_3 substrates. The transition loss is about 1 dB at 60 GHz. Bias voltages are fed through hermetically sealed feed-through-pins. A metal cap has a fine screw placed above the DR for mechanical tuning of the oscillation frequency. The package size excluding the flange is $20.5 \times 8.5 \times 5$ mm^3 or 0.9 cc.

Fig. 16 shows frequency-control characteristics together with output power against the control voltage input. The modulation sensitivity is 11.5 MHz/V, which was adjusted using an attenuator in order to have good interface matching with the nominal input voltage of the Ethernet signal. The output power was also regulated so as to be matched to the system specification of 10 dBm. The measured value is 10.2 dBm at 59.5 GHz. The phase noise is -71 dBc/Hz at 100 kHz off-carrier. This is worse than that for the MMIC VCO itself, because the 4 V supply voltage of the VCO is lower

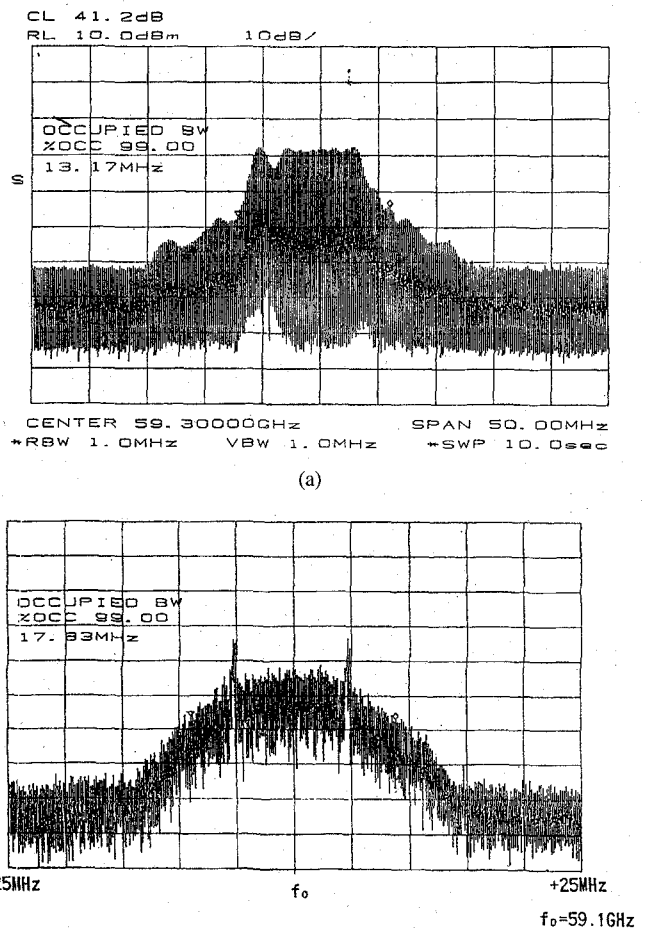

Fig. 18. Modulation spectra of the transmitter module. (a) FM: NTSC test-pattern signal input. (b) FSK: 10 Mbps digital signal input.

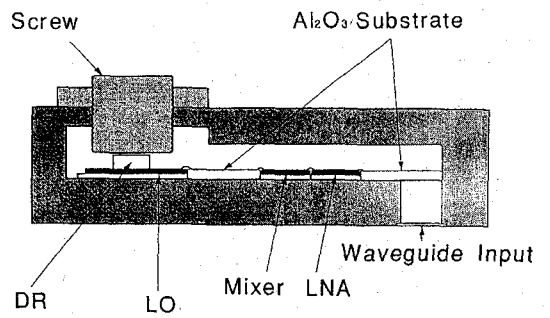

Fig. 19. Schematic diagram of the receiver module; cross-sectional view.

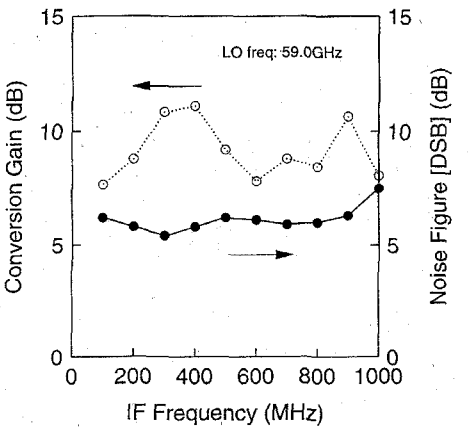

Fig. 20. Receiver-module noise figure and conversion-gain variations with IF.

than the phase-noise optimum value of 5 V and because the DR location is optimized for stability rather than for minimum phase noise. Fig. 17 shows the temperature dependence of the frequency and output power. The temperature coefficient of the frequency is −2.4 ppm/°C. The frequency stability is ±36 ppm for an ambient temperature range of 25 ±15°C. The output power deviation of ±0.6 dB is also small. The oscillation frequency can be mechanically tuned from 58.2–60.1 GHz, completely covering the Japanese experimental band from 59–60 GHz. The dc power consumption is 0.8 W.

The high-speed modulation capability of the transmitter module was demonstrated. Fig. 18(a) and (b) are FM and FSK modulation spectra with the NTSC test-pattern signal input and 10 Mbps digital signal input, respectively. Good modulation with an index of one can be seen. These results indicate that this transmitter module is very promising for practical indoor use.

B. Receiver Module

A receiver module was fabrricated using a similar package, assembling an LNA, a mixer, and an LO chip as shown in Fig. 19. Fig. 20 shows the IF frequency dependence of the noise figure and conversion gain. The local frequency is 59.0 GHz. A conversion gain of 9.2 dB with a 6.2 dB double-side band (DSB) noise figure has been obtained at 59.5 GHz RF and 500 MHz IF. The best noise figure is 5.4 dB with a 10.8 dB conversion gain at 300 MHz IF. The dc power consumption is 0.39 W. The LO frequency can be mechanically tuned from 58.4 to 59.8 GHz.

These T/R modules have been proven to be applicable to high-speed wireless LAN systems with more than 10 Mbps data rate, and video-signal and compressed HDTV-signal (MUSE) transmission systems [28]. The 60 GHz-band monolithic DR-stabilized oscillators are effective to realize these ultra-miniature transmitter/receiver modules for practical use.

V. Conclusion

Ultra-miniature FM/FSK transmitter/receiver modules utilizing a complete MMIC chip set including DR-stabilized fundamental-frequency oscillators for multimedia wireless communication systems at 60 GHz-band have been developed. The MMIC's have been realized using 0.15-μm gate N–AlGaAs/InGaAs/N–AlGaAs DH-HJFET's as active elements and a drain dc-biased HJFET as an integrated varactor. The 0.9 cc transmitter module, which consists of a VCO and two power-amplifiers, exhibits an 11.5 MHz/V modulation sensitivity and 10.2 dBm of output power with a −2.4 ppm/°C frequency stability. The receiver module, which consists of an LNA, a mixer, and an LO, has a 5.4 dB DSB noise figure with a 10.8 dB downconversion gain for 300 MHz IF. The 60 GHz-band monolithic DR-stabilized oscillators

are effective in realizing ultra-miniature transmitter/receiver modules for practical high-speed wireless LAN systems and video-signal transmission systems.

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